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DE-10 Super Expansion Board

For Terasic DE-10 Nano FPGA boards

Assembly & Technical Information Manual

Manual v1.0

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Introduction

Thank you for purchasing the DE-10 Super Expansion Board! This is device will expand the capabilities of the Terasic DE-10 Nano FPGA developer board. This board is also compatible with popular "MiSTer project" cores.

Installation Requirements

The included heat sink is placed on top of the DE-10 Nano FPGA developer board's FPGA chip. The DE-10 Super Expansion Board then simply installs on top of the DE-10 Nano FPGA developer board.

Warranty Information

This product carries a limited lifetime warranty. Units subject to improper installation, misuse, abuse, or modifications will not be covered under this warranty. We may at our discretion either repair or replace the unit covered under warranty. The customer will pay all freight charges to and from our facility. cbmstuff.com must be contacted to obtain a return authorization. Any product returned without authorization will be returned without repair or replacement.

Liability

By using this product you agree to hold cbmstuff.com and Jim Drew free from any type of liability either directly or indirectly while using this product.

Legal Information

The 'look and feel' and functionality of this product are protected by U.S. copyright laws. Various terminology and feature names are protected under U.S. trademark laws.

SECTION 1 – INSTALLATION

Locate the included heat sink and heat sink tape. The heat sink tape is double-sided, so there is adhesive on both sides. Remove the cover from one side of the heat sink tape and place it centered on the heat sink. Remove the cover from the other side of the heat sink tape. Orient the heat sink so that the cooling fins are parallel to the long connectors, and place it centered as best as possible directly over top of the FPGA chip and press the heat sink down onto the FPGA chip. DO NOT PRESS TOO HARD! See Figure 1 for details.

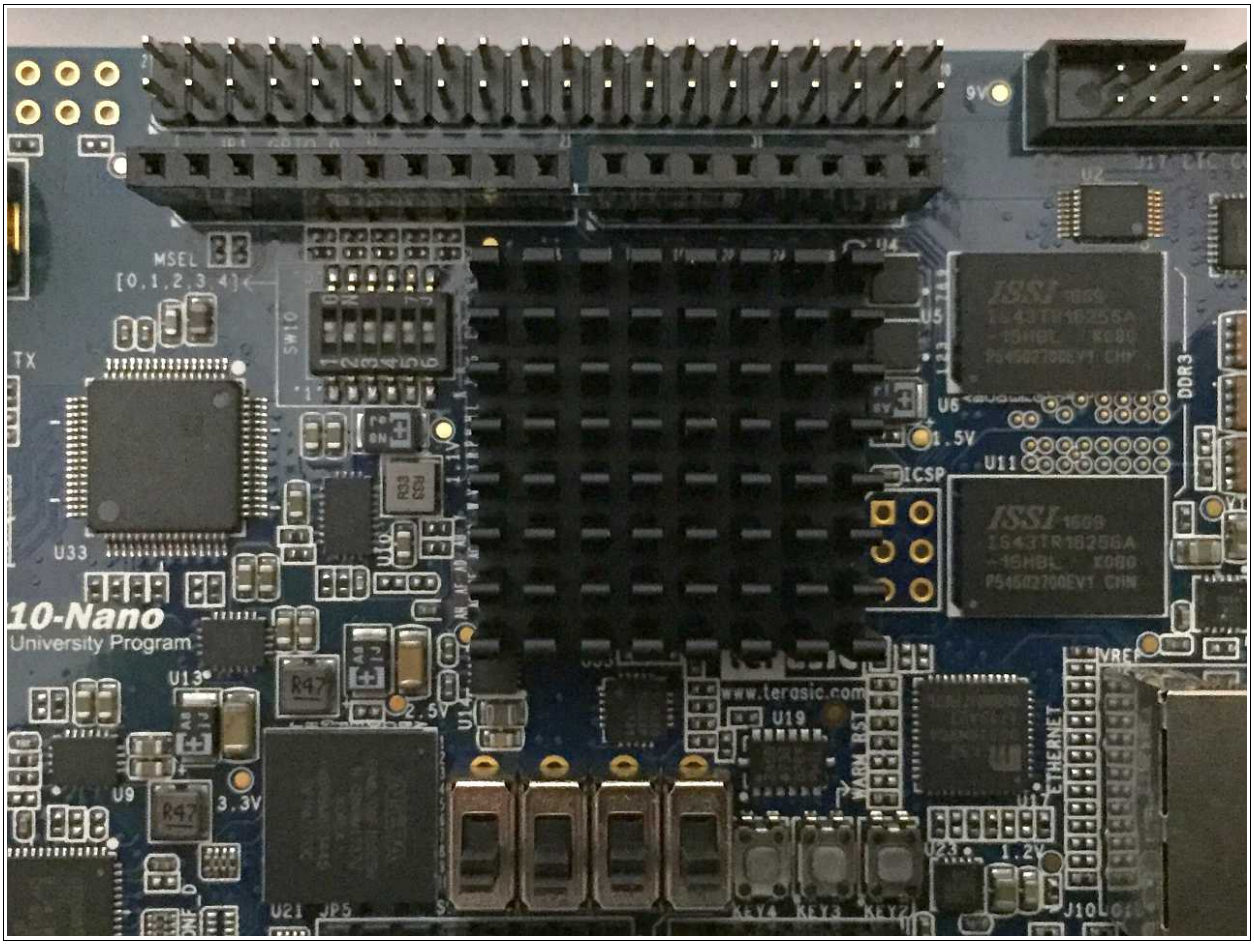


Figure 1 – Heat sink mounted on FPGA chip

The DE-10 Super Expansion Board has numerous connection points. It is important that you pay attention to those points during assembly.

Orient the DE-10 Super Expansion Board over top of the DE-10 Nano FPGA developer board so that the connectors and four corner holes all line up. See Figure 2 for details. Slowly press the two boards together straight, not at an angle, making sure that the internal pins and LTC bridge connector pins are going into their sockets. Refer to Figure 3. Continue to press the boards together until the four corners are flush with the mounting posts. When the boards are fully together you can put screws (that came with the DE-10 Nano FPGA developer board) into each corner and tighten them. The screws are not necessary. See Figure 4 for the completed assembly.

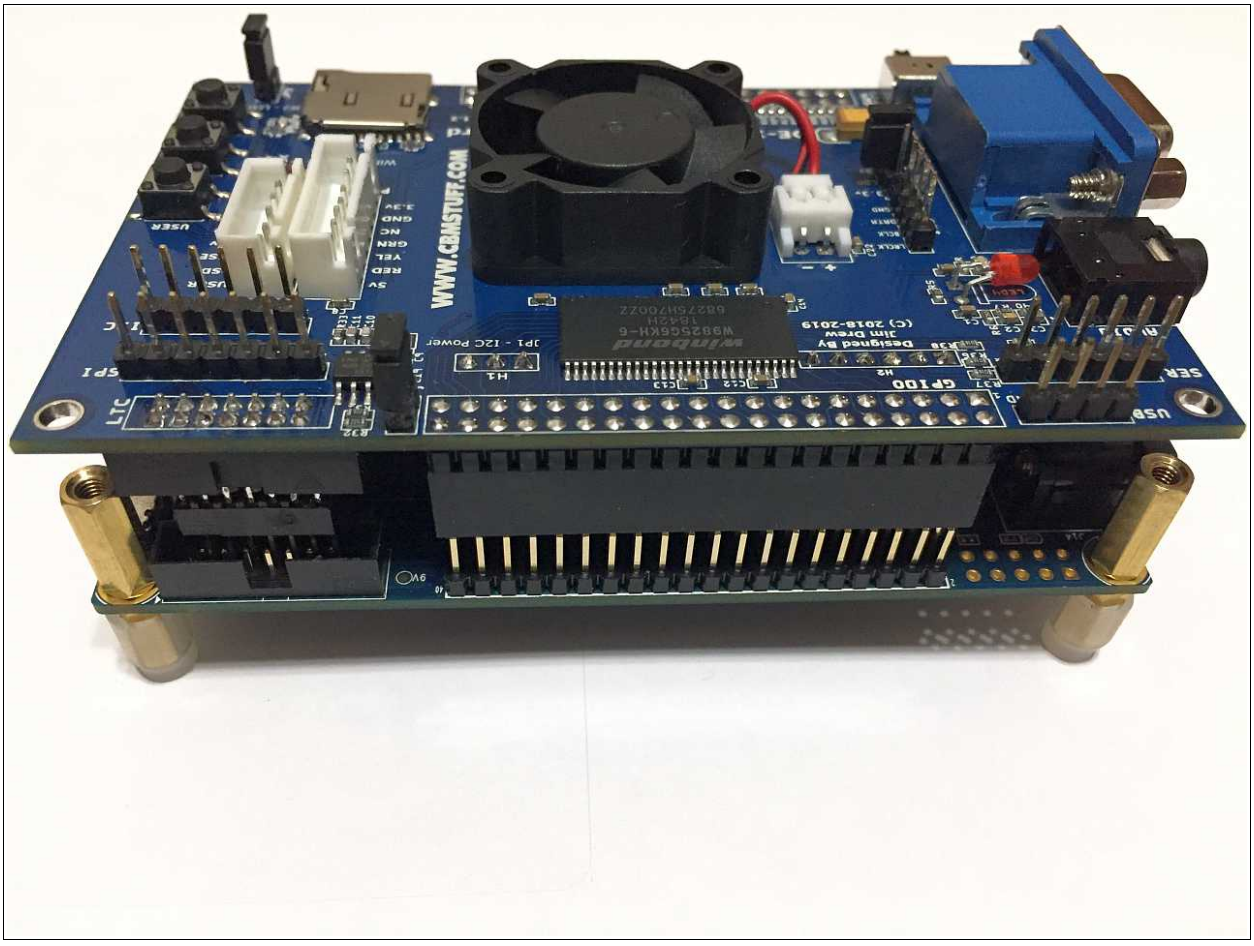


Figure 2 – Orientation of boards

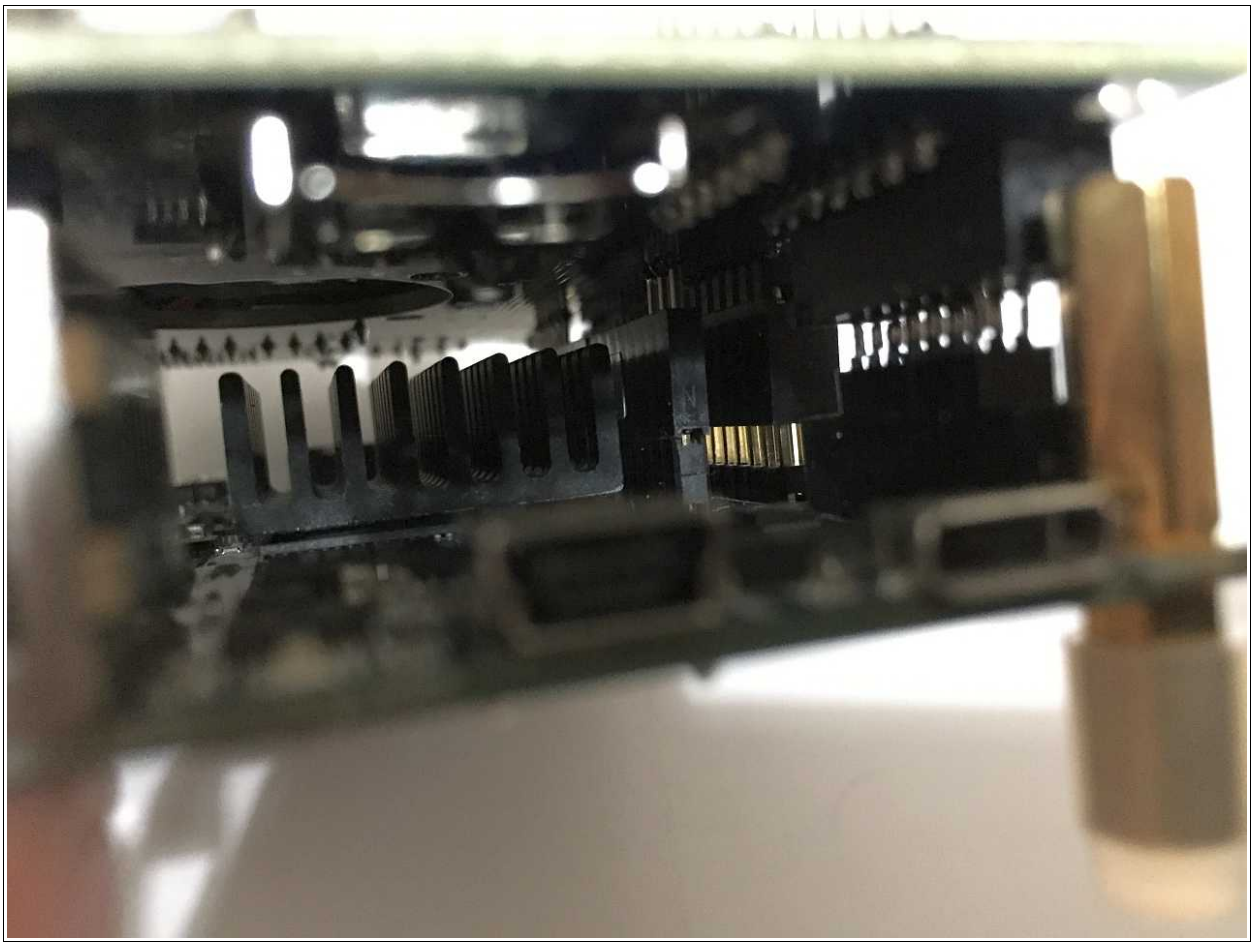


Figure 3 – Internal pin alignment

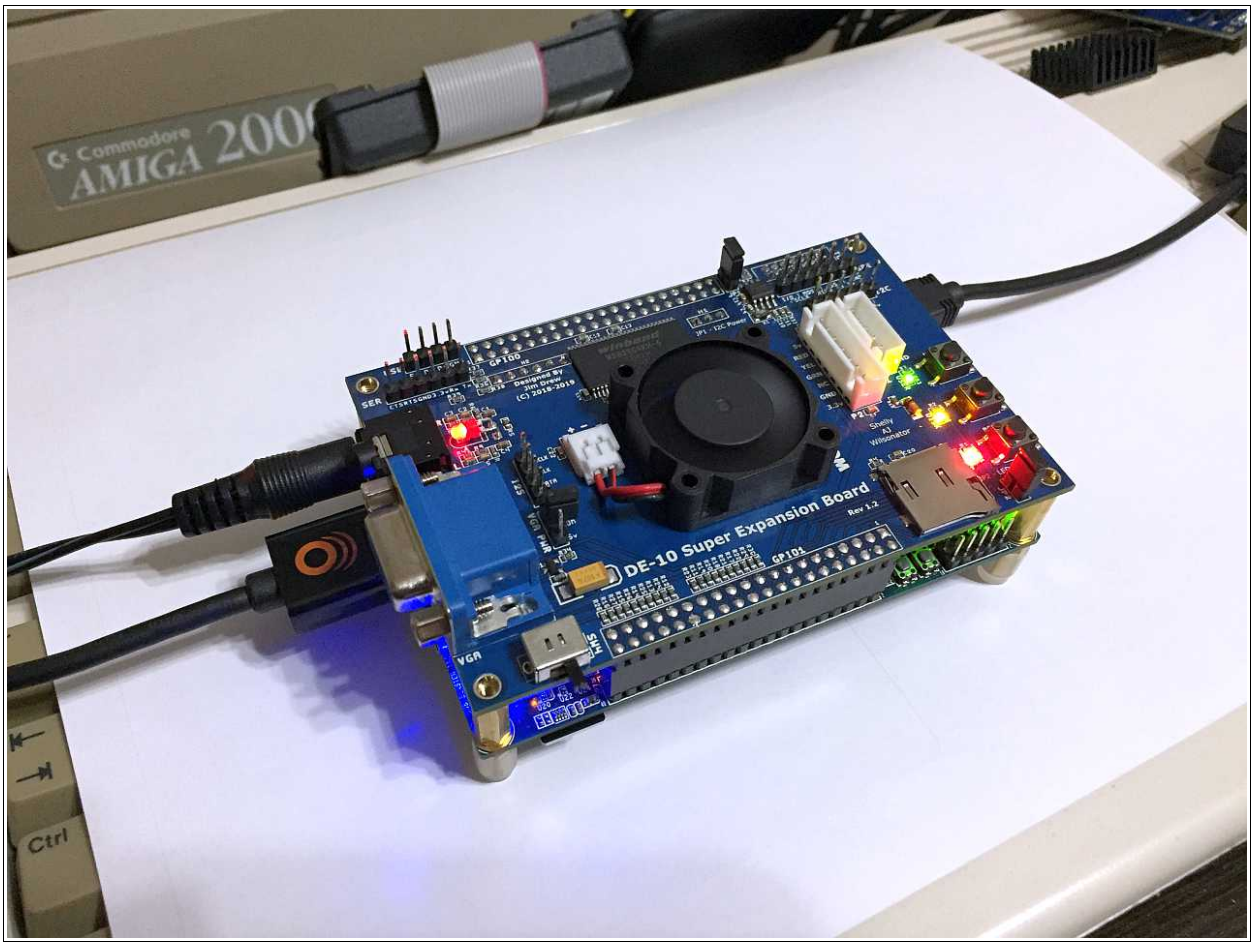


Figure 4 – Assembled setup

SECTION 2 – INFORMATION

The DE-10 Super Expansion Board provides many features for the FPGA developer. See SECTION 3 for all connection details. Feature list:

SDRAM

32MB of SDRAM is connected directly to the FPGA chip.

Real time clock

A Microchip MCP79410 real time clock (RTC) chip. The RTC is battery backed-up using a 1220 series coin cell battery. There are 4.7K pull-up resistors on the SDA and SCL lines when jumper JP1 is in place. When JP1 is removed, there are no pull-up resistors on these lines.

The MCP79410 has 64 bytes of battery backed up SRAM, 1Kb of EEPROM, and a 64 bit OTP protected UID that is blank by default. This can be used for permanent storage of MAC address or other similar permanent UID.

The RTC chip is connected to the LTC connector. See Microchip's datasheet for the MCP79410 for function details.

Micro-SD card socket

A micro-SD card socket is connected directly to the FPGA chip.

SPI and I2C break out headers

The LTC connector is passed through and broken into two separate headers to provide SPI and I2C ports for expansion purposes. The RTC chip is connected to the RTC port.

Audio and TOSLink outputs

A stereo 3.5mm audio jack is connected to the FPGA chip through a 30Hz/12KHz band-pass filter. A single 3mm LED is connected directly to the FPGA chip to provide a TOSLink output.

Switches and LEDs

There are three normally-open push button switches and three LEDs connected directly to the FPGA chip.

VGA Output

The VGA output is connected to three 6-bit linear R2R ladders to provide a 18 bit (6-6-6) DAC color output. The each leg of the resistor ladder is connected directly to the FPGA chip.

Separate HSYNC and VSYNC signals are driven directly by the FPGA chip.

A SOG (sync-on-green) circuit allows compatibility with old VGA/EGA monitors that require this feature controlled through SW4.

MiSTer compatibility

The SDRAM, VGA, Micro-SD, audio, and RTC are all pin compatible with the various MiSTer project cores. The MiSTer project info can be found here:

https://github.com/MiSTer-devel/Main_MiSTer/wiki

SECTION 3 – PIN ASSIGNMENTS

This section describes the pin assignments for all of the components, headers, jumpers, switches, and connectors.

Header H1 pin assignments

Pin No.	FPGA Pin No.	Description	Arduino Feature	I/O Standard
1	PIN_AG10	Arduino IO2	General I/O	3.3-V
2	PIN_AF13	Arduino IO1	TXD	3.3-V
3	PIN_AG13	Arduino IO0	RXD	3.3-V

Header H2 pin assignments

Pin No.	FPGA Pin No.	Description	Arduino Feature	I/O Standard
1	PIN_AG11	Arduino IO15	SCL	3.3-V
2	PIN_AH9	Arduino IO14	SDA	3.3-V
3	No Connection	No Connection		
4	Ground	Ground	Ground	Ground
5	PIN_AH12	Arduino IO13	SCK	3.3-V
6	PIN_AH11	Arduino IO12	MISO	3.3-V

Header SER pin assignments

Pin No.	FPGA Pin No.	Description	MiSTer Feature	I/O Standard
1	PIN_AH9	Arduino IO15	Tx	3.3-V
2	PIN_AG11	Arduino IO14	Rx	3.3-V
3	3.3V	3.3V	3.3V	3.3V
4	Ground	Ground	Ground	Ground
5	PIN_AH12	Arduino IO13	RTS	3.3-V
6	PIN_AH11	Arduino IO12	CTS	3.3-V

Header USB pin assignments

Pin No.	FPGA Pin No.	Description	MiSTer Feature	I/O Standard
1	Ground	Ground	Ground	Ground
2	PIN_AH9	Arduino IO15	D+	3.3-V
3	PIN_AG11	Arduino IO14	D-	3.3-V
4	5V	5V	5V	5V

Header SPI pin assignments

Pin No.	LTC Pin No.	Description	SPI Feature	I/O Standard
1	3,8,13	Ground	Ground	Ground
2	2,10	3.3V	3.3V	3.3-V
3	6	LTC SS	SS	3.3-V
4	5	LTC MISO	MISO	3.3-V
5	7	LTC MOSI	MOSI	3.3-V
6	4	LTC SCLK	SCLK	3.3-V
7	14	LTC I/O	I/O	3.3-V

Header I2C pin assignments

Pin No.	LTC Pin No.	Description	I2C Feature	I/O Standard
1	1	9V	9V	9V
2	9	LTC SDA	SDA	3.3-V
3	11	LTC SCL	SCL	3.3-V
4	3,8,13	Ground	Ground	Ground
5	2,10	3.3V	3.3V	3.3-V
6	NA	5v	5V	5V

Header I2S pin assignments

Pin No.	FPGA Pin No.	Description	MiSTer Feature	I/O Standard
1	PIN_AG26	SPDIF/LRCLK	LRCLK	3.3-V
2	PIN_AC24	AUDIO_L/BCLK	BCLK	3.3-V
3	PIN_AE25	AUDIO_R/DATA	DATA	3.3-V
1	Ground	Ground	Ground	Ground

Header P1 pin assignments

Pin No.	FPGA Pin No.	Description	Feature
1	Ground	Ground	Ground
2	3.3V	3.3V	3.3V
3	PIN_AG23	RESET button	RESET button (SW1 via diode)
4	PIN_AG25	OSD button	OSD button (SW2)
5	PIN_AH24	USER button	USER button (SW3)

Header P2 pin assignments

Pin No.	FPGA Pin No.	Description	Feature
1	3.3V	3.3V	3.3V
2	Ground	Ground	Ground
3	No connection	No connection	No connection
4	PIN_Y15	Green LED	POWER LED (LED3)
5	PIN_AA15	Yellow LED	DISK LED (LED2)
6	PIN_AG28	Red LED	POWER LED (LED1)
7	5V	5V	5V

Jumper VGA PWR pin assignments

Pin No.	Description	Feature
1	5V	5V
2	COM	VGA power
3	3.3V	3.3V

Jumper JP1 pin assignments

Pin No.	Description	Feature
1	3.3V	3.3V
2	I2C Power	I2C Pull-up resistor power

Jumper JP2 pin assignments

Pin No.	Description	Feature
1	3.3V	3.3V
2	LED Power	Power for internal LEDs

Switch USER pin assignments

Pin No.	FPGA Pin No.	Description	MiSTer Feature	I/O Standard
1,2	PIN_AH24	SW3	USER switch	3.3-V
3,4	Ground	Ground	Ground	Ground

Switch OSD pin assignments

Pin No.	FPGA Pin No.	Description	MiSTer Feature	I/O Standard
1,2	PIN_AG25	SW2	OSD switch	3.3-V
3,4	Ground	Ground	Ground	Ground

Switch RESET pin assignments

Pin No.	FPGA Pin No.	Description	MiSTer Feature	I/O Standard
1,2	PIN_AG23	SW1 1 (via diode)	RESET switch	3.3-V
3,4	Ground	Ground	Ground	Ground

Connector VGA pin assignments

Pin No.	Description
1	Red signal
2	Green signal
3	Blue signal
4	No connection
5	Ground
6	Ground
7	Ground
8	Ground
9	VGA PWR COM
10	Ground
11	No connection
12	No connection
13	HSYNC
14	VSYNC
15	No connection

Connector FAN pin assignments

Pin No.	Description	Feature
1	5V	5V
2	Ground	Ground

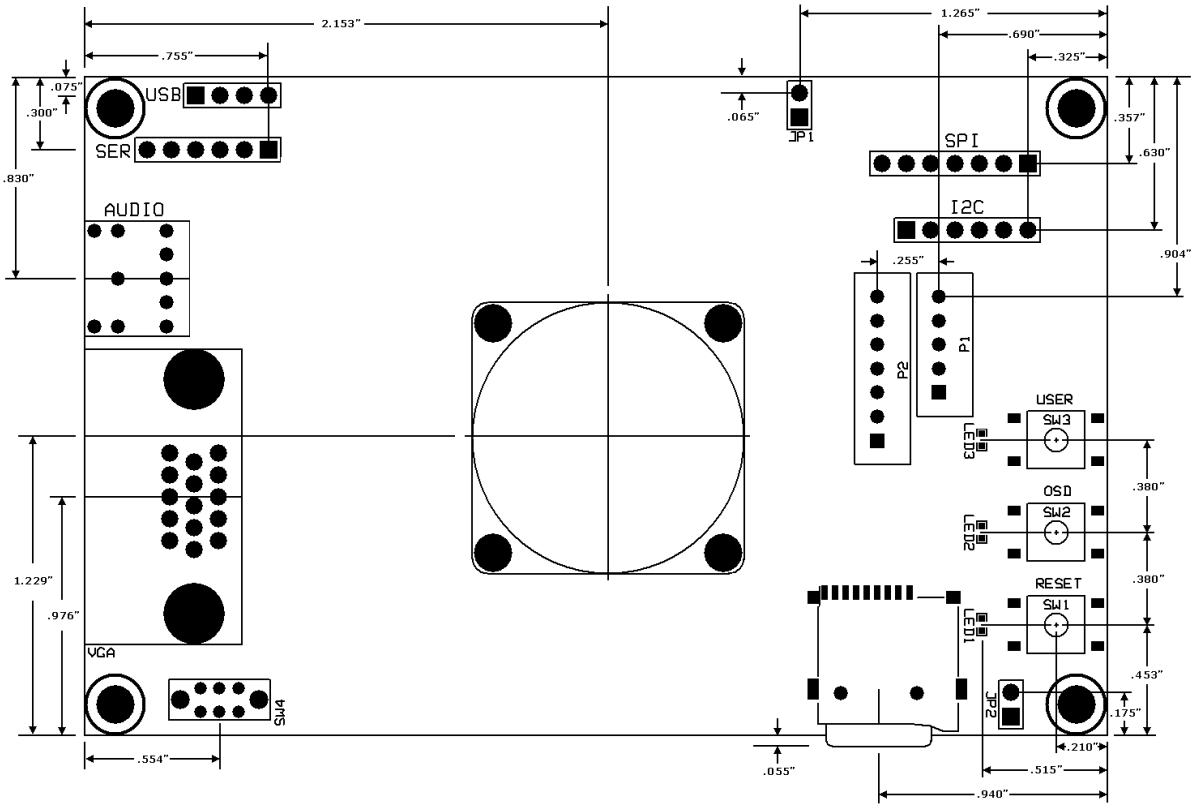
SDRAM pin assignments

Pin No.	FPGA Pin No.	SDRAM Signal
1	3.3V	3.3V
2	PIN_E8	DQ0
3	3.3V	3.3V
4	PIN_V12	DQ1
5	PIN_D11	DQ2
6	Ground	Ground
7	PIN_W12	DQ3
8	PIN_AH13	DQ4
9	3.3V	3.3V
10	PIN_D8	DQ5
11	PIN_AF4	DQ6
12	Ground	Ground
13	PIN_AF7	DQ7
14	3.3V	3.3V
15	PIN_AG13	LDQM
16	PIN_AA19	/WE
17	PIN_AA18	/CAS
18	PIN_W14	/RAS
19	PIN_Y18	/CS
20	PIN_Y17	BS0
21	PIN_AB25	BS1
22	PIN_AB26	A10
23	PIN_Y11	A0
24	PIN_AA26	A1
25	PIN_AA13	A2
26	PIN_AA11	A3
27	3.3V	3.3V

SDRAM pin assignments (continued)

Pin No.	FPGA Pin No.	SDRAM Signal
28	Ground	Ground
29	PIN_W11	A4
30	PIN_Y19	A5
31	PIN_AB23	A6
32	PIN_AC23	A7
33	PIN_AC22	A8
34	PIN_C12	A9
35	PIN_AD17	A11
36	PIN_D12	A12
37	PIN_AG10	CKE
38	PIN_AD20	CLK
39	PIN_AF13	UDQM
40	No connection	No connection
41	Ground	Ground
42	PIN_AE24	DQ8
43	3.3V	3.3V
44	PIN_AD23	DQ9
45	PIN_AE6	DQ10
46	Ground	Ground
47	PIN_AE23	DQ11
48	PIN_AG14	DQ12
49	3.3V	3.3V
50	PIN_AD5	DQ13
51	PIN_AF4	DQ14
52	Ground	Ground
53	PIN_AH3	DQ15
54	Ground	Ground

SECTION 4 – MECHANICAL DRAWING



SECTION 5 – COMPLIANCY

The enclosed device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (*i.*) this device may not cause harmful interference and (*ii.*) this device must accept any interference received, including interference that may cause undesired operation.